20-Gb/s Digital SSI's Using AlGaAs/GaAs Heterojunction Bipolar Transistors for Future Optical Transmission Systems

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Abstract— **Design principles to achieve good eye opening and circuit optimization to extract high performance from AlGaAs/GaAs HBT devices are described. Using the circuit techniques and HBT's with an f_T of 70 GHz and an f_{max} of 50 GHz, four kinds of SSI's are developed for future optical transmission systems. High-bit-rate operation of over 20 Gb/s (26-GHz toggle flip-flop, 20-Gb/s decision circuit, 20-Gb/s EXCLUSIVE OR/NOR gate, and 28-Gb/s selector IC), extremely fast rise and fall times (20–80%) of 20 and 14 ps, respectively, and good eye opening are obtained. In addition, potential performance gains that might be realized through advanced circuit and device design are appraised, and throughputs as fast as 40 Gb/s are predicted.**

I. Introduction

VERY-high-speed optical transmission systems using single-mode optical fiber and intensity modulation are expected to play important roles in future broad-band and integrated services digital networks. Recently, a number of optical transmission experiments have been carried out at bit rates exceeding 10 Gb/s [1], [2]. Very-high-speed electronics are indispensable to realize such high-speed systems that offer high reliability, cost-effectiveness, and compactness. What is more, the application of optical transmission systems is a key motivator that is driving the development of high-speed devices and IC technologies. The question naturally arises what kind of devices should be applied to realize these high-speed IC's, and intensive efforts are underway to develop high-speed IC's operating at 10 Gb/s using Si bipolar transistors [3], GaAs MESFET's [4], [5], MISFET's [6], and HBT's [7], [8]. Recently a number of IC's that operate at speeds exceeding 20 Gb/s have also been reported [9]–[11].

In terms of high-speed performance, the AlGaAs/GaAs HBT is one of the promising candidates, because it combines the advantages of the high transconductance of bipolar devices and the high-speed electron mobility of compound materials. Devices with f_T or f_{max} values of more than 100 GHz have been reported [11], [12]. In specific IC applications, very fast speeds are being reported for many applications: a divided operating up to 36 GHz [13], a 30-Gb/s 2 : 1 multiplexer [14], among others.

Building on these recent results, we have developed four kinds of digital IC's using HBT's that operate at more than 20 Gb/s for optical communication applications. Two of these IC's have been described previously [10], [15], and the remaining two are described here for the first time. This paper describes the circuit design, design principles, and optimization to extract the best performance from currently available AlGaAs/GaAs HBT technology and to realize IC's for practical applications. Beyond this, the paper looks ahead and makes educated projections on the likely performance of HBT IC's on the basis of fabricated IC performance. We will be particularly concerned with the likely speed performance that will be achieved using AlGaAs/GaAs HBT's.

Section II focuses on circuit design, design principles, and circuit optimization. Section III describes the IC performances of four fabricated circuits that yield throughputs in excess of 20 Gb/s. Finally, Section IV gives our prognosis of performance levels that are likely to be reached based on evolving device performance and circuit technology trends.

II. Circuit Design

A. Design Principles

The following design principles were adopted to achieve good eye opening and to make the IC's user-friendly.

1) Single-ended inputs and outputs with logic swing of 1 V are used for chip-to-chip interfaces. Within the chip, differential drive signals are employed with voltage swings of 500 mV. To achieve high-speed performance, differential inputs and outputs with voltage swings of 500 mV confer inherent advantages [3], [16]. However, pair interconnections between chips make system assembly more complicated than if single interconnections were employed. Thus, single-ended input to the chip and differential operation inside the chip are essential to simplify system assembly and to keep the high-speed operation at the same time. The logic swing of 1 V for the single-ended input and 500 mV for the differential operation is necessary to obtain sufficient voltage gain and voltage margin as will be described later in detail. High and low levels at the interface are 0 and −1 V, respectively, which are common values for the open collector level of Si bipolar IC's and the open drain level of GaAs-MESFET SCFL circuits that are in widespread use.

2) A current-switch output driver with collector outputs is used to reshape the waveform and to achieve fast rise and fall times. Collector outputs were first adopted instead of emitter-follower outputs to reach bit rates up to a few gigabits per second [17], [18] and this approach must be

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IEEE Log Number 9204737.

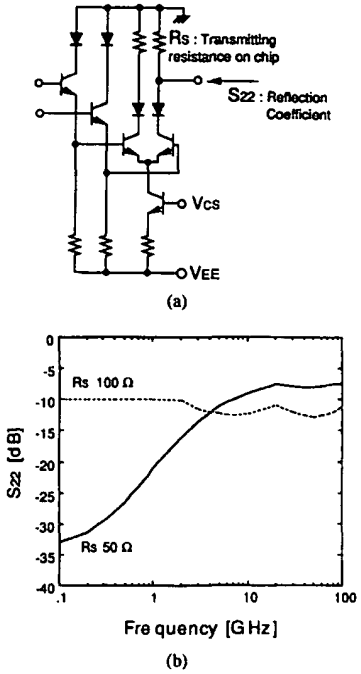


Fig. 1. (a) Circuit configuration of output current switch with transmitting resistances. (b) Simulated reflection coefficients.

adopted for bit rates exceeding 10 Gb/s in conjunction with following impedance matching. The driver switches a large output current of 30 mA to generate output voltage swings of 1 V in the case of impedance matching at both the receiving and transmitting ends described below.

3) Fifty-ohm input termination resistors at the receiving ends and 100-Ω output termination resistors at the transmitting ends are integrated on-chip to reduce time jitter and waveform distortion resulting from multiple reflections. The 50-Ω input resistors are connected to the base of the input emitter followers in the conventional way. This receiving-end configuration can guarantee good matching as the frequencies approach the f_T of the transistor, since the bandwidth of the emitter follower is the same order of f_T as the transistor [19]. At transmitting ends, the effect of the transistor capacitances is not low, since the termination resistors are set to the diodes at the collector sides of the output current switch as shown in Fig. 1(a). These diodes are used to reduce breakdown concerns and to optimize f_T. This means that 50 Ω may not be the optimum value in the high-frequency region. Simulated reflection coefficients for the configuration shown in Fig. 1(a) for 50- and 100-Ω termination resistors are presented in Fig. 1(b). The S_{22} for 100 Ω is lower than that for 50 Ω in the frequency range beyond 4 GHz, since the impedance of transistor capacitances affects the results. Thus, 100-Ω termination resistors are adopted at the transmitting ends.

Measured reflection coefficients at the receiving end, S_{11}, and at the transmitting end, S_{22}, of the fabricated HBT IC are shown in Fig. 2. An S_{11} of −20 dB at 10 GHz (corresponding to 20 Gb/s in NRZ data) and −15 dB at 20 GHz (corresponding

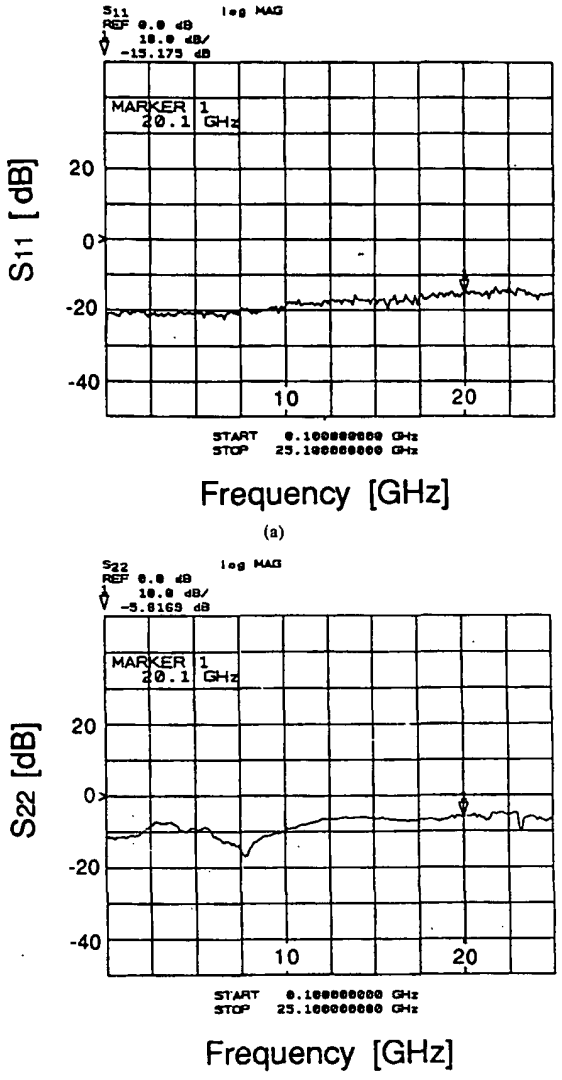


Fig. 2. Measured reflection coefficients: (a) receiving end, and (b) transmitting end.

to 40 Gb/s in NRZ data), and an S_{22} of −10 dB at 10 GHz and −6 dB at 20 GHz were obtained. The dc level at which S_{11} and S_{22} were simulated and measured is the center of the logic level.

4) A single supply voltage of −7 V is used. Reference voltage V_{REF} and current-source voltage V_{CS} are generated on chip for the simple system assembly.

B. Circuit Optimization

For circuit optimization, we were guided by the following considerations to achieve high speed and good eye opening. Note that high input sensitivity is also important, because this represents one of the chief advantages of bipolar devices over GaAs MESFET devices. Optimization procedures are compared with those of Si bipolar IC's.

1) Optimization of current density transistors is the most crucial factor to achieve high speed. In the case of Si bipolar devices, the transistor cutoff frequency f_T, a dominant factor determining speed characteristics, should increase with increasing current density in the low current density region. Beyond a critical current density in the high-current-density region, however, f_T would decrease with increasing current density due to the base-widening effect. In addition, f_T also has a strong dependence on V_{CE}. This means that to optimize the current density of individual transistors, the f_T dependence on J_C and V_{CE} should be taken into account. Thus, an accurate transistor model that expresses these characteristics is indispensable [20], [21]. For high-speed design, the J_C's of transistors are set beyond the point yielding the maximum f_T.

In our HBT, the upper current density is limited by a different factor. Because of the rather large emitter resistance compared with Si bipolar devices, the voltage gain is reduced in the high-current-density region due to the emitter resistance-induced serial feedback effect. Current density dependence of the simulated voltage gain of a fundamental ECL gate and measured f_T are depicted in Fig. 3. In the region $J_C \geq 5\times10^4$ A/cm^2, f_T continues to increase as J_C increases. However, the voltage gain falls below 0 dB in the region. Obviously, this means that ECL digital circuits cannot operate in the region because the voltage gain is insufficient. Thus, the optimum current density is lower than the point that yields the maximum f_T, in this case less than half the level that gives the maximum f_T. In other words, under the condition of maintaining the same load resistance and the same dc current in the current source, the larger transistors guarantee the sufficient voltage gain for ECL operation. This is because the larger transistors have smaller parasitic emitter resistance. However, increasing transistor size while maintaining the operating current reduces the operating current density and associated f_T. To sum up the discussion so far, the trade-off between voltage gain and f_T should be taken into account in optimizing the current density. The voltage gain reflects the sensitivity of the circuit, and the f_T reflects the speed performance. Thus, our approach has been to optimize the current densities of all parts of the circuits according to whether sensitivity or speed was the more important consideration. To illustrate, the design current density of a preamplifier is shown together with that of a D-latch in the decision circuit in Fig. 3. As shown in the figure, the J_C of the amplifier, 2.5×10^4 A/cm^2, is set lower than that of the D-latch, 5×10^4 A/cm^2, because the amplifier requires higher input sensitivity and the D-latch requires faster speed.

In addition, the special dependence of f_T on V_{CE} in HBT's has also been modeled in a simple and straightforward manner [22].

2) Optimization of the internal voltage swing is done considering the trade-off between voltage margin and speed. The measured transfer characteristics of a current switch with 1-V input and 1-V output are depicted in Fig. 4. Solid lines show the transfer curves for the central current density of 2.5×10^4 A/cm^2, and dashed lines those of 5×10^4 A/cm^2. Transfer widths of 300 mV for the former and 400 mV for the latter were obtained. One would expect these results given the large emitter resistance. The values are quite large

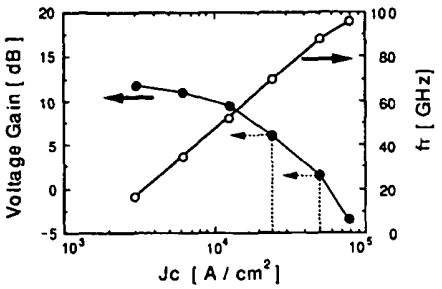


Fig. 3. Voltage gain of ECL gate and f_T versus current density of the transistors.

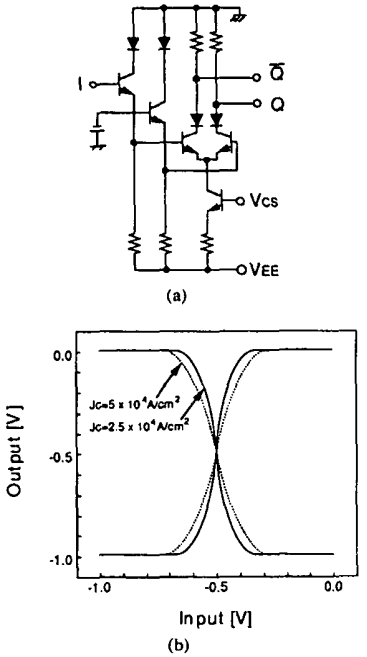


Fig. 4. Transfer characteristics of ECL gate: (a) circuit configuration, and (b) dc transfer characteristics.

in comparison with about 150 mV for Si bipolar devices. Therefore, the voltage swing in the present HBT cannot be reduced to the voltage swing widely used in Si bipolar IC's. Simulated results indicate that the toggle-flip/flop circuit with internal voltage swing of less than 300 mV could not operate due to insufficient gain. Therefore, a differential internal voltage swing of 500 $mV_{p\text{-}p}$ is used to achieve sufficient voltage margins as well as high speed. The value is larger than that of Si bipolar devices by a factor of 2.

3) Si bipolar IC's generally adopt two-stage emitter followers in D-latches for high-speed applications [3]; here we adopt one-stage emitter followers in the D-latches. This was done to minimize the supply voltage and to boost the speed performance. This is because the base–emitter voltage of an HBT is quite high, up to 1.5 V, and the f_T decreases with increasing V_{CE}. Two-stage emitter followers have only been employed for clock input level shifting and for driving 30 mA through the output current switch because of the large driving capability.

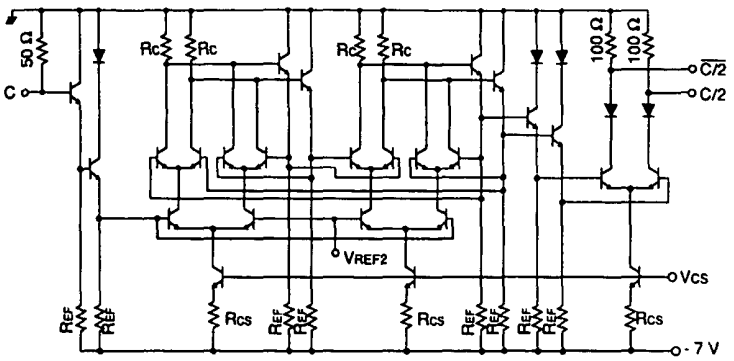


Fig. 5. Circuit configuration of T-F/F.

III. SSI's Performance

Based on the design considerations described in Section II, four kinds of IC's for application to future optical transmission systems were designed and fabricated. A self-aligned AlGaAs/GaAs HBT technology was used, which satisfies our speed and yield requirements [23]. The current gain cutoff frequency f_T is 70 GHz, and the maximum oscillation frequency f_{max} is 50 GHz at the J_C of 2.5×10^4 A/cm^2. Most of the HBT's have an emitter size of 2×5 μm. In this section, performances of the four fabricated IC's are described. All IC's were tested on the wafer using RF probes.

A. Toggle Flip/Flop

The toggle flip/flop (T-F/F) is key in synchronizing the data processing between two different bit-rate channels in optical transmission systems. The maximum operating speed of T-F/F's is one limiting factor of such systems. The circuit configuration of the T-F/F is shown in Fig. 5. A two-level ECL series-gating technique was adopted. In this configuration, maximum operating frequency is about $1/(2t'_{pd})$, where t'_{pd} is the delay time of the upper current switch in the series gate and is 1.5–2.0 times larger than that of the basic gate. To reduce the t'_{pd}, current density of the upper current switch should be increased. In contrast to the decision circuit that we will consider the next, for the T-F/F we are more concerned with speed than sensitivity. Here, therefore, the current density of the upper differential pairs has been increased to 5×10^4 A/cm^2 as described in Fig. 3.

Measured input sensitivity and output amplitude versus input frequency are shown in Fig. 6. Very-high-speed operation with a self-oscillation frequency of 20 GHz and a maximum operating frequency of 26 GHz were obtained. In addition, the input sensitivity of 5–21 GHz is less than 300 $mV_{p\text{-}p}$, and the output amplitude up to 24 GHz is more than 800 $mV_{p\text{-}p}$. The input sensitivity is not very high for a bipolar device, but it is sufficient for transmission applications.

Input and output waveforms at 10 and 23 GHz are shown in Fig. 7. Very clean output waveforms were obtained with very short rise and fall times (20–80%) of 25 and 15 ps, respectively. The power dissipation was 945 mW.

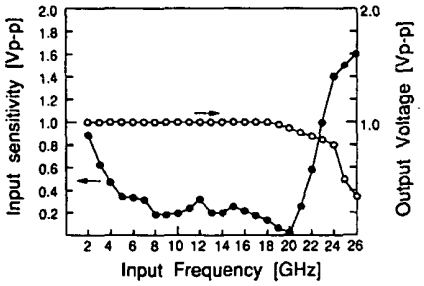


Fig. 6. Measured input sensitivity and output amplitude versus input frequency.

B. Decision Circuit

The decision circuit follows amplifier stages in the receiver, and is employed to restore small analog input signals and to regenerate digital signals by retiming. Since both high input sensitivity and retiming operations are required, a D-latch circuit configuration with preamplifier is best suited. The circuit configuration is basically the same as that reported previously [22] as shown in Fig. 8. It consists of a wide-band parallel feedback preamplifier, an internal buffer, a D-latch, and an output buffer. To realize both high speed and high input sensitivity, the current densities of the amplifier and the D-latch were optimized individually as described earlier in Section II-B.

To measure the decision ambiguity width, a pseudorandom pattern generator and an error detector were used up to 10 Gb/s. To measure bit rates over 10 Gb/s, the measuring system described in [22] was utilized. Employing this latter system, a pseudorandom NRZ signal up to 20 Gb/s was generated and error-free operation up to 20 Gb/s was confirmed. The input data were $2^{15} - 1$ length pseudorandom sequence NRZ signals and the bit error rate was less than 1×10^{-9}.

The measured decision ambiguity width and the clock phase margin are shown in Fig. 9. Ambiguity widths of 25 mV at 10 Gb/s and 720 mV at 20 Gb/s were obtained. The clock phase margin were 260° at 10 Gb/s and 6° at 20 Gb/s. Error-free operation up to 20 Gb/s was confirmed. The input and output eye patterns at a bit rate of 20 Gb/s are shown in Fig. 10. While the input pattern was fairly sinusoidal-like and

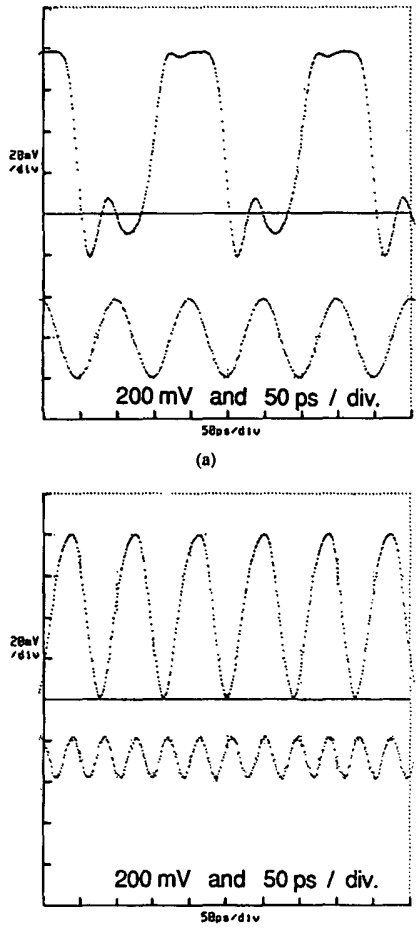


Fig. 7. Input and output waveforms of T-F/F: (a) 10 GHz and (b) 23 GHz.

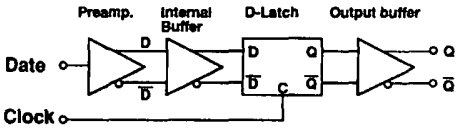


Fig. 8. Block diagram of decision circuit.

contained time jitter, the regenerated output pattern was pulse-like and exhibited much less jitter. Good eye opening was obtained. The power dissipation was 1120 mW.

Using this decision circuit IC, 20-Gb/s signal transmission was carried out [24].

C. EXCLUSIVE-OR/NOR

The EXCLUSIVE-OR/NOR (XOR) gate is a key component for signal processing in optical transmission systems. Its applications include differentiation and full-wave rectification, coded mark inversion (CMI) coding, and differential mark inversion (DMI). The circuit configuration of the XOR IC is shown in Fig. 11. It consists of an input level-shift stage of emitter followers, an internal XOR core stage using a two-level series gating technique, an output driver stage, and a bias-generating stage that is not shown in the figure.

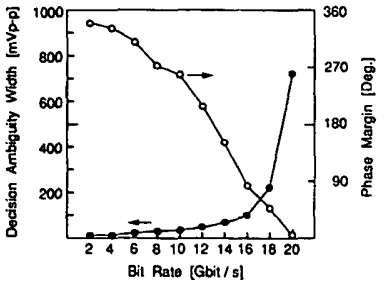


Fig. 9. Measured decision ambiguity width and clock phase margin versus bit rate.

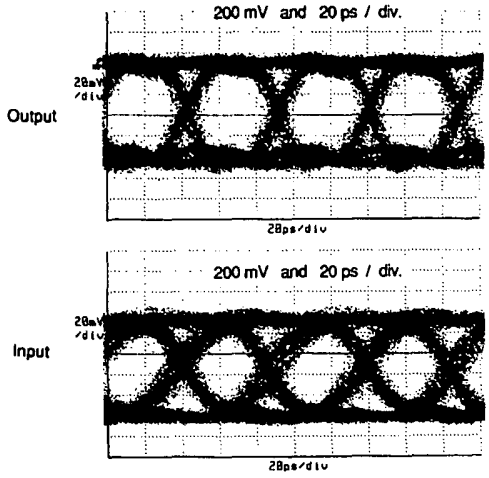


Fig. 10. Input and output eye patterns at 20 Gb/s of the decision circuit.

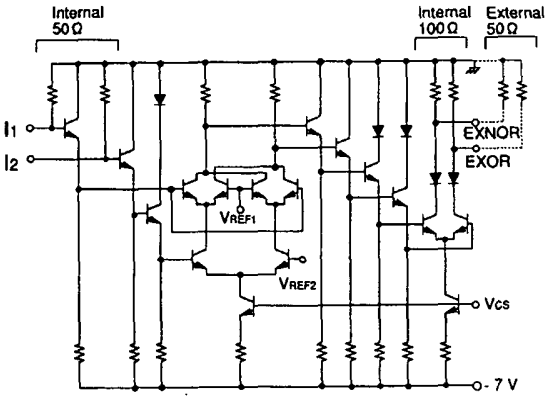
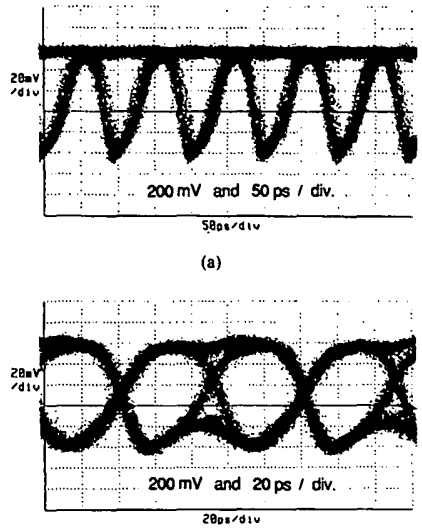


Fig. 11. Circuit configuration of EXCLUSIVE OR/NOR gate.

Fig. 12(a) shows the output pattern when both inputs are driven by equal pulse sequences at 10 Gb/s, one of which is shifted in phase by half a bit width from the other. The XOR is adopted to perform the differentiation and full-wave rectification of a pulse sequence in clock recovery circuits. The pattern shows the 10-GHz frequency characteristics clearly.



(a)

(b)

Fig. 12. Output eye patterns. (a) Output pattern when inputs are driven by 10-Gb/s pulse sequence shifted from each other by half a bit. (b) Output dipulse pattern at 20 Gb/s.

Next, Fig. 12(b) shows the so-called dipulse pattern at 20 Gb/s when one input is driven by a 10-Gb/s NRZ sequence and the other by a 10-GHz clock signal. A satisfactory voltage swing of 1 V was obtained. Extremely fast rise and fall times (20–80%) of 22 and 14 ps, respectively, as well as good eye opening, were achieved. In addition, the time jitter is quite small. The pattern demonstrates the IC can operate as fast as 20 Gb/s. Power dissipation was 700 mW.

D. Selector

The time-division multiplexer (MUX) is a key component in transmitters. It combines several parallel data channels to a single data sequence with optical transmission speeds. In this paper, the selector means the core part of the MUX and does not have input and output retiming D-F/F's. The selector can achieve higher speeds than the MUX with retiming D-F/F's, because the input clock frequency of the selector is only half that of the MUX. In practical applications, however, the MUX is the device of choice, because time jitter should be reduced in front of the optical device as much as possible. Thus, the main task of the selector is to generate faster bit streams than have been available in order to measure newly developed IC's and perform transmission experiments.

A block diagram of the selector IC is depicted in Fig. 13. It consists of input buffer gates, a selector gate, and an output driver. It should be noted that the clock buffer is added because the clock frequency is half that of the output bit rate. The clock buffer is thus not a limiting factor of the IC and is necessary to achieve good eye opening.

The selector IC was tested under the condition that the $D2$ input was inverted and shifted several bits in relation to the $D1$ input. Fig. 14(a) shows the output patterns at 22 Gb/s when the operating speed of the pattern generator is boosted to 11 Gb/s using an external clock. A very sharp and clean eye pattern

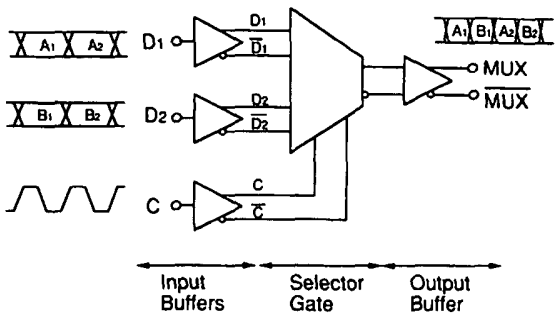
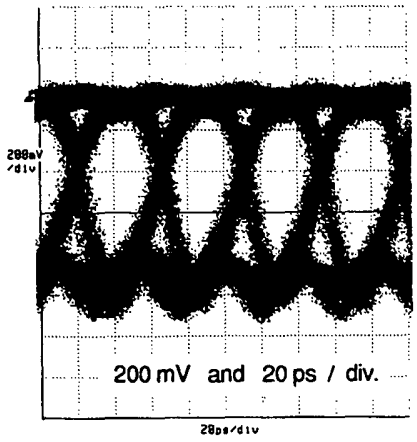
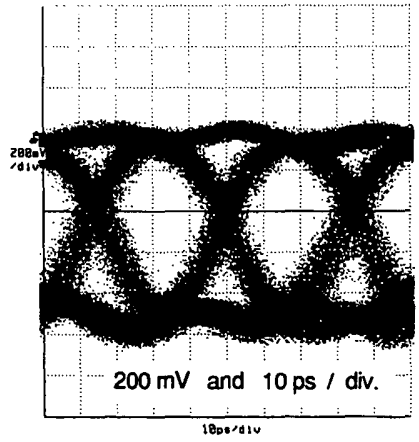


Fig. 13. Block diagram of selector IC.



(a)



(a)

Fig. 14. Output eye patterns of the selector IC: (a) 22 Gb/s and (b) 28 Gb/s.

was obtained. A sufficient voltage swing of 1 $V_{p\text{-}p}$ and rise and fall times (20–80%) of 20 and 16 ps, respectively, were achieved at 22 Gb/s. Fig. 14(b) shows the output patterns at 28 Gb/s, where the data arrived at 7 Gb/s and the clock at 14 GHz. The output voltage was slightly reduced due to the bandwidth of the output driver. Here too, however, good eye opening was obtained. Power dissipation was 1050 mW.

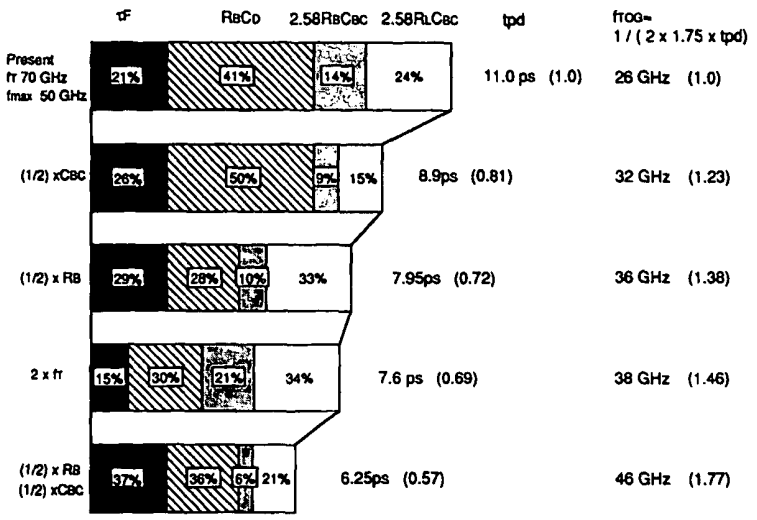


Fig. 15. Components of basic gate delay of the present and future AlGaAs/GaAs HBT and expected maximum toggle frequencies.

IV. Discussion

In the preceding section it was shown that high-bit-rate operations of over 20 Gb/s were obtained for the fabricated HBT IC's using the practical design principles outlined in Section II and the HBT device described briefly in Section III. High throughput operation of up to near 30 Gb/s was realized for the NRZ data signal from the performance of the selector IC, while 20-Gb/s operation was possible for the clock signal from the performance of the decision circuit. It is obvious that the clock path in the circuits would constitute a limit on the circuits' performance.

To achieve even higher speed operation, what aspects of circuit and device design should be improved upon? First, concerning the circuit design, we might anticipate a fair improvement in performance, if some of the restrictions on system assembly could be relaxed. For example, simulation results indicate that changing the clock signal interface from dc coupled to ac coupled with 500-mV differential driving for the direct connecting lower current switch of ECL series gates could yield 20% faster operation. Moreover, if the internal voltage swing could be boosted to 250 mV by reducing the emitter resistance, this should yield an overall improvement in performance on the order of 30%.

In a number of special applications, particular circuit configurations can be exploited to achieve substantial gains in performance [16]. For example, a parallel approach might be applied to decision circuits [25], and regenerative frequency division could be useful for dividers [26], [27] and circuits using the divider. These techniques could potentially push maximum bit-rate operations up by about 50%.

What aspects or features of device design should be optimized to obtain higher bit rates? The relation between basic gate delay and device parameters is clarified by the following analytical equation [28]:

$$t_{pd} = \tau_F + R_B C_D + 2.58 R_B C_{BC} + 2.58 R_L C_{BC}$$

where $\tau_F = 1/(2\pi f_T)$ is the transit time, R_B is the base resistance, $C_D = I_C \tau_F / 0.15$ is the diffusion capacitance, C_{BC} is the base–collector junction capacitance, and R_L is the load resistance of the ECL gate.

The implications of the equation are graphically shown in Fig. 15. The value of 11 ps derived by the equation is in good agreement with the 9.8 ps derived by circuit simulation. The percentage of each time constant is also shown. The time constant $R_B C_D$ is 41% of the total delay and is the largest component. Furthermore, the time constant resulting from τ_F (or f_T) is $\tau_F + R_B C_D$ and occupies 62% of the total delay. With this procedure, we find that the time constant from R_B is $R_B C_D + 2.58 R_B C_{BC}$ (55% of the total delay), and the time constant from C_{BC} is $2.58 R_B C_{BC} + 2.58 R_L C_{BC}$ (38% of the total delay). It is thus clear that f_T, R_B, and C_{BC} are the dominant factors in that order.

Although obviously each parameter could not be improved independently of the other parameters in an actual device context, here we have attempted to do just that to see what insights might be gained regarding improvement trends. The delay times for half of C_{BC}, half of R_B, double f_T, and half of R_B and C_{BC} are also shown in Fig. 15. Reducing C_{BC} makes the gate delay 20% faster, and reducing R_B or increasing f_T makes the gate delay about 30% faster. Moreover, reducing both R_B and C_{BC} makes the delay 40% faster. Turning to the bit rate, the t'_{pd} of the upper current switch with a fan-in/fan-out of 2 in the T-F/F is conveniently assumed to be larger than the t_{pd} by 1.75. Since the maximum operating frequency of the T-F/F is approximately given by $1/(2t'_{pd})$, 26 GHz is obtained where $t_{pd} = 11$ ps, which is equal to the measured value of the T-F/F. Employing this relation, the expected maximum frequencies f_{TOG}'s are shown in Fig. 15. Reducing both R_B and C_{BC} makes it possible to achieve a bit rate of 40 GHz or more.

The advanced performance of HBT described here is not unrealistic, because an f_T of about 160 GHz [12] and an $f_{\max}$

of more than 200 GHz [29] have already been reported. At the same time, it should also be noted that these high performances should be realized in the range where voltage gain reduction by the emitter resistance is negligible. Reduction of the emitter resistance to maintain voltage gain or reduction of junction capacitances to achieve high f_T and f_{max} in relatively low current density are important considerations.

V. Conclusion

This paper focuses on practical circuit design to extract superior performance using currently available AlGaAs/GaAs HBT technology. Key design principles and optimization procedures were discussed in comparison with Si bipolar IC's. Based on the circuit design concepts presented, four kinds of IC's were fabricated and high-bit-rate operation of more than 20 Gb/s was verified. More specifically, we demonstrated a 26-GHz T-F/F, a 20-Gb/s decision circuit, a 20-Gb/s EXCLUSIVE-OR/NOR gate, and a 28-Gb/s selector IC. We were thus able to verify that the circuit design principles do actually yield 20-Gb/s operation.

Another aim of the paper was to review the future prospects for performance enhancement of AlGaAs/GaAs HBT IC's based on experimental results. By enhancing device parameters and by pushing the technology to its limits through aggressive circuit design, it should be possible to achieve throughputs of 40 Gb/s. While making this optimistic prediction, certain reservations should also be noted. First, even to realize a 10-Gb/s IC module, packaging is a serious limiting factor that should be taken into account in circuit design [5]. Second, how to assemble and measure the performance of devices are serious obstacles that might be addressed. Finally, since the wire length in chips is equal to 1/4 wavelength at 40 Gb/s, conventional lumped-element design may not be feasible. It goes without saying that all these problems must be squarely faced and solutions found before 40-Gb/s IC's can be realized and applied.

Acknowledgment

The author wishes to thank Y. Yamauchi for help with device characterization, O. Nakajima, K. Nagata, and T. Nittno for device fabrication, and K. Hagimoto, Y. Miyamoto, and M. Ohata for providing measurement tools. The author also wishes to thank M. Suzuki, N. Ieda, and M. Hirayama for their encouragement.

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